A Monolithic 2-V 950-MHz CMOS Bandpass Amplifier with A Notch Filter for Wireless Receivers

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Abstract **- A fully-integrated 950-MHz bandpass amplifier for use in a wireless receiver is designed in a standard 0.5-μm CMOS process. A Q-compensation circuit is embedded to achieve a desired bandwidth of 25 MHz. Unbalanced g_m-cells are used to maximize the linearity. A notch filter is adopted to achieve an image rejection of 50 dB. A switchable-capacitor array is used to tune the center frequency over 100 MHz range. The amplifier measures a gain of 22 dB with an IIP3 of -17 dBm, a noise figure of 10 dB and draws a current of 25 mA from a 2-V supply.**

I. INTRODUCTION

Typically, a heterodyne wireless receiver requires an image rejection of around 80 dB. Due to phase mismatch and amplitude mismatch, image-rejection mixers can provide only up to 30 dB image rejection. Another 50 dB image rejection should be provided by an RF bandpass filter. Off-chip SAW filters are excellent and normally used for this purpose, but they are bulky and cannot be integrated on the same chip. To save the power, to reduce the size, and to enable single-chip integration, on-chip RF bandpass filters with high image rejection are needed.

In this paper, a CMOS RF bandpass amplifier with a notch filter to be used in a wireless receiver, as shown in Fig. 1, is presented. This amplifier can provide an image rejection of 50 dB and a gain of 22 dB for frequencies around 950 MHz with a narrow bandwidth of 25 MHz, which corresponds to a high Q of 38.

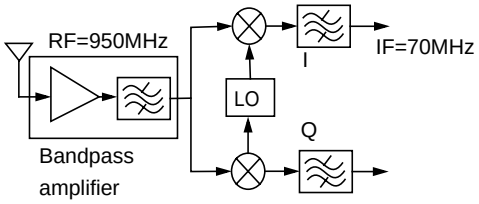

Fig. 1. Use of the Proposed Bandpass Amplifier in a Wireless Receiver

II. AMPLIFIER DESIGN

As shown in Fig. 2, the proposed bandpass amplifier includes two stages. The first stage is a cascode differential pair with inductive input matching [1] and an LC resonant tank as the output loading. Inductor degeneration is used to obtain the input matching because it can achieve better noise performance than $1/g_m$ or resistive termination. C_{gs} of the input devices are made as small as possible to minimize the noise figure [2].

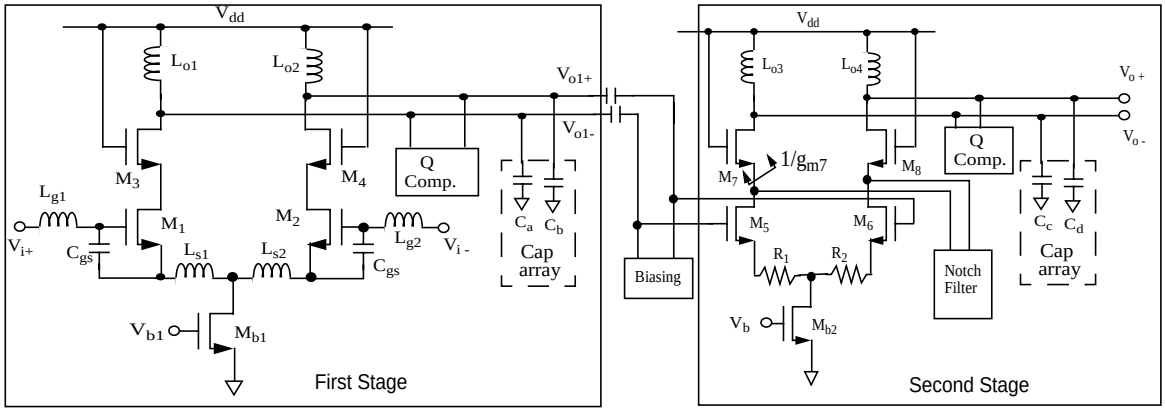

Fig. 2. Schematic of the Proposed Bandpass Amplifier

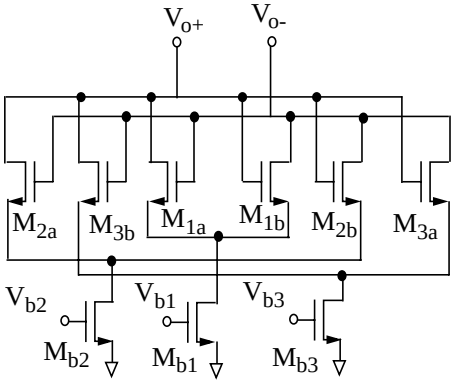

Fig. 3. Schematic of the Q-Compensation Circuit

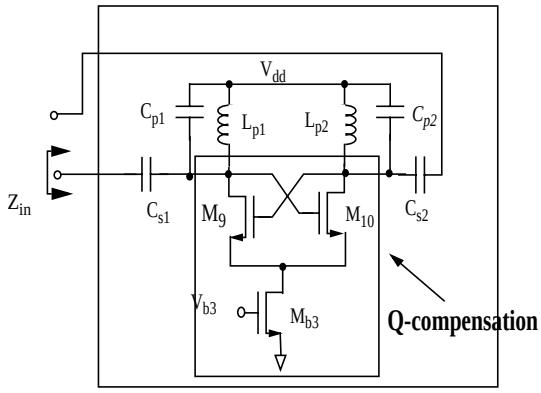

Fig. 4. Schematic of the Proposed Notch Filter

To compensate for the low Q of the output spiral inductor, which is as low as 2.5, to achieve the desired bandwidth of 25 MHz, a Q-compensation circuit with negative G_m is introduced, as shown in Fig. 3. It is a simple differential pair with two pairs of unbalanced g_m-cells. M_{1a} - M_{1b} provides most of the negative G_m. However, it drops when output voltage V_{o+}-V_{o-} is large. Unbalanced g_m-cells, M_{2a}-M_{2b} and M_{3a}-M_{3b}, are used to provide extra current to maintain a constant g_m over a wide range of V_{o+}-V_{o-}. Therefore, better linearity of the whole amplifier is achieved with unbalanced g_m-cells [3].

The second stage of the amplifier has basically the same architecture as that of first stage but with resistive source degeneration to minimize the chip area. The noise from the resistors, R_1 and R_2, is negligible when referred to the input of the whole amplifier due to the high gain of the first stage. Capacitor coupling is used between the two stages to enable operation at a 2-V supply.

The two-stage combination yields a fourth-order bandpass function with a bandwidth of 25 MHz but can provide only 27-dB image rejection at 140 MHz offset. A notch filter is adopted in the second stage to achieve an overall image rejection of 50 dB. To minimize the overall noise figure, the gain of first stage is set to a high value of 22 dB, and that of second stage is 0 dB. The center frequencies of the two stages are slightly deviated from each other to obtain maximum image rejection.

III. Notch Filter

A second-order notch filter was first demonstrated in a cascode LNA for image rejection [5]. However, such a notch filter can only control the response at the image frequency.

Fig. 4 shows the schematic of the notch filter used in this design. A third-order notch filter [6] is used because of its ability of controlling the frequencies at both the image and the desired signals separately. A Q-compensation circuit is used to compensate the loss in the low-Q on-chip inductors, L_{p1} and L_{p2}. The input impedance (Z_{in}) looking into the filter can be written as

$$Z_{in}(s) = \frac{L_p(C_s + C_p)\cdot s^2 + 1}{C_s C_p L_p \cdot s^3 + C_s \cdot s} \qquad (1)$$

At the desired signal frequency, the impedance looking into the notch filter is much higher than $1/g_{m7}$ (as shown in Fig. 2) such that no ac current will be drawn away from the original path. At the image frequency, the impedance looking into the notch filter is low such that all image current will be 'stolen' from the original signal path. As a result, the suppression at the image frequency is effectively increased, and the gain at the desired frequency is not affected.

The ability of image rejection depends on the difference of impedance between the notch filter and the original bandpass amplifier, $1/g_{m7}$, at the image frequency. The larger the difference, the higher the image rejection is. The notch filter is employed at the second stage instead of the first stage of the bandpass amplifier because the second stage has lower input g_m and thus its cascode devices have higher impedance. At the same time, the noise contributed by the notch filter can be further decreased by the gain of first stage.

IV. Frequency-Tuning Circuitry

In previous work [3], a Miller capacitor is used to tune

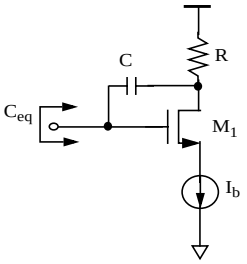

Fig. 5. Miller Capacitor Used in Previous Design [3]

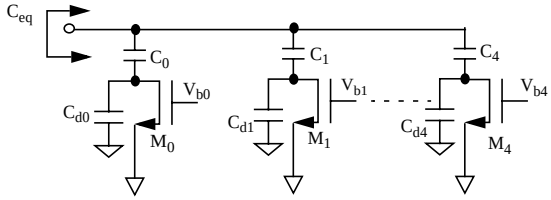

Fig. 6. Switchable-Capacitor Array Proposed for Frequency Tuning

the center frequency, as shown in Fig. 5. By tuning the g_m of the transistor, M_1, the equivalent capacitance can be varied. However, extra noise is introduced from the transistor M_1 and the resistor R. In addition, M_1 degrades the overall linearity and consumes extra power.

To avoid these problems, a 5-bit binary-weighted switchable-capacitor array [4] is used in this design as shown in Fig. 6. The parasitic drain capacitor C_{d0} - C_{d4} of the transistors limits the capacitance tuning range and therefore the frequency tuning range. To minimize the drain capacitance to achieve a maximum tuning rage, donut transistors are used in realizing M_0 - M_4 [4]. With these transistors, a frequency tuning range of more than 100 MHz can be obtained. The turn-on resistors of M_0 - M_4 limit the overall Q of the capacitor array. To maximize the Q, a larger size for M_0 - M_4 is more desirable. However, the tuning range will be degraded due to the larger parasitic drain capacitance. To trade off between the Q and the capacitance tuning range, the size of transistors are properly set so that the overall capacitor can maintain a Q of 10. Because the noise is dominated by the low Q of on-chip inductor, which is about 2.5, the noise contribution of switchable-capacitor array is negligible. Moreover, their linearity is good, and they consume no DC power.

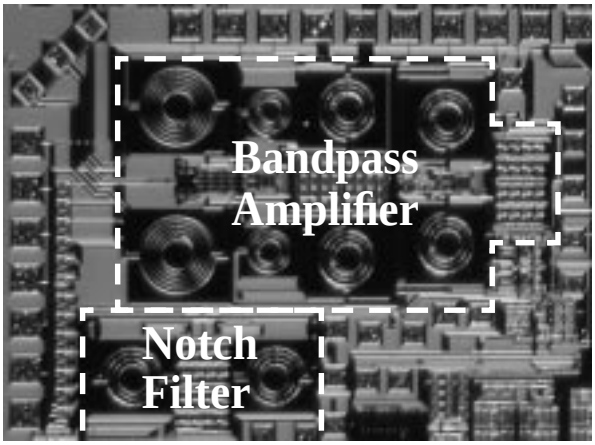

Fig. 7. Die Photo of the Complete Bandpass Amplifier

V. Experimental Results

The complete bandpass amplifier has been fabricated in a standard 0.5-μm CMOS process. The die photo of the amplifier is shown in Fig. 7, and the chip area is 1.5 mm^2.

The measured input matching, S11 of the amplifier is shown in Fig. 8. Due to the high parasitic capacitance of the gate inductor, the center frequency of the S11 is shifted to lower frequency. However, it can still achieve S11 of -10 dB at the desired frequency.

The measured frequency response of the complete 2-stage bandpass amplifier is shown in Fig. 9. With the enhancement from the notch filter, the amplifier can achieve a maximum image rejection of 50 dB at 140 MHz offset. The gain is measured to be 22 dB.

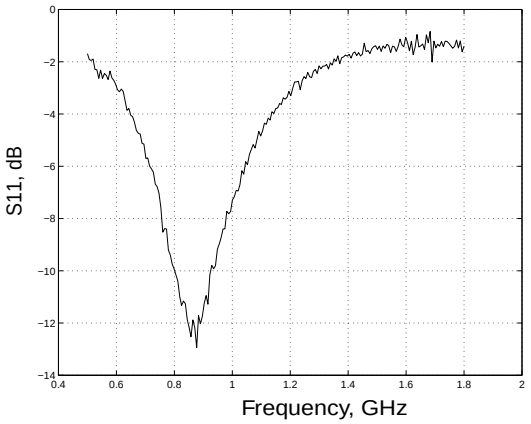

Fig. 8. Measured Input Matching, S11

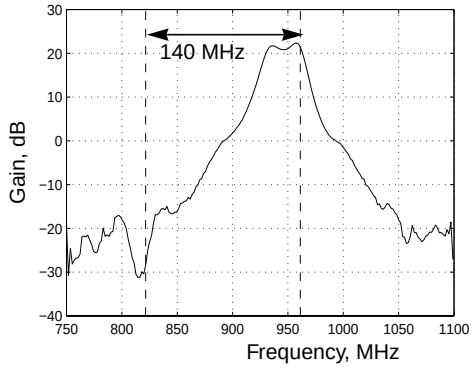

Fig. 9. Measured Frequency Response of the Amplifier

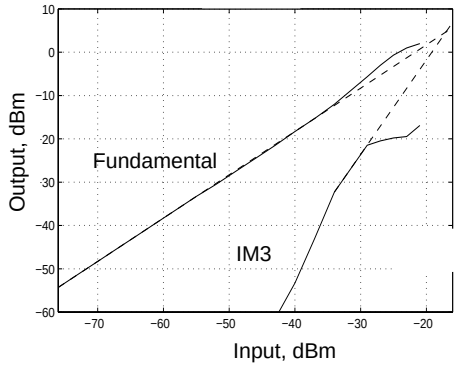

Fig. 10. Two-Tone Measurement of the Amplifier

The two-tone measurement result is shown in Fig. 10. Two input signals are located at 800 KHz away from each other. The IIP3 is measured to be -17 dBm. The noise figure is 10 dB, which is dominated by the low-Q on-chip inductors used for input matching. The measurement results are summarized in Table I.

VI. Conclusion

A monolithic 2-V RF bandpass amplifier with a notch filter to be used in wireless receivers is demonstrated. With the notch filter, the image rejection is achieved to be 50 dB, which is sufficient to eliminate the use of an off-chip image-rejection RF filter. The desired bandwidth of 25 MHz which corresponds to a high Q of 38 is achieved by compensating the loss of the on-chip inductors using negative g_m-cells. Unbalanced g_m-cells are used to maximize the linearity.

Fabricated in a 0.5-μm CMOS process, the gain and the IIP3 are measured to be 22 dB and -17 dBm, respectively. With the switchable-capacitor array, the frequency tuning range is more than 100 MHz. The measured noise figure is 10 dB, which is dominated by the loss due to the on-chip inductors for the input matching. The amplifier consumes a total current of 25 mA from a 2-V single supply and occupies a total chip area of 1.5mm^2.

TABLE I Summary of Measurement Results

Parameters	Performance
Technology	0.5-μm CMOS
Gain	22 dB
Center Frequency	947 MHz
Bandwidth	25 MHz
Q	38
Image rejection	50 dB
IIP3	-17 dBm
NF	10 dB
V_{dd}	2 V
Current	25 mA
Chip Area	1.5 mm^2

References

[1] Derek K. Shaeffer, Thomas H. Lee, “A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier”, *IEEE Journal of Solid-Stage Circuits*, Vol. 32, No. 5, pp 745 - 759, May 1997.

[2] Giovanni Girlando and Giuseppe Palmisamo, “Noise Figure and Impedance Matching in RF Cascode Amplifiers”, *IEEE Transactions on Circuits and Systems*, Vol. 46, No. 11, pp 1388 - 1396, Nov. 1999.

[3] David Leung and Howard Luong, “A Fourth-Order CMOS Bandpass Amplifier with High Linearity and High Image Rejection for GSM Receivers”, *Proceedings of IEEE International Symposium on Circuit and Systems 1999*, Florida, USA, pp. 589-592, June 1999.

[4] Chi-Wa Lo and H. Luong, “A 1.5-V 900-MHz Monolithic CMOS Fast-Switching Frequency Synthesizer for Wireless Applications”, *Symposium on VLSI Circuits 2000*, Hawaii, USA, June 2000, to appear.

[5] J. A. Macedo and M. A. Copeland, “A 1.9 GHz Silicon Receiver With Monolithic Image Filtering”, *IEEE Journal of Solid-State Circuits*, VOl. 33, No. 3, pp 378 - 386, March 1998.

[6] H. Samavati, H. R. Rategh, T. H. Lee, “A 12.4 mW CMOS front-end for a 5 GHz wireless-LAN receiver”, *Symposium on VLSI Circuits*, Appl. Phys. 1999, pp.87-90. Tokyo, Japan.